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Sheet 1 of 4

MysSrsForm PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2506	PRIORITY SERIAL NO. 10/364,710
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Arup Bhattacharyya	
				PRIORITY FILING DATE February 10, 2003	GROUP 2814 Unknown
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	AB		Yamauchi, N. et al., "Drastically Improved Performance in Poly-Si TFTs with Channel Dimensions Comparable to Grain Size", IEDM Tech. Digest, 1989, pp. 353-356.		
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	AJ		Gu, J. et al., "High Performance Sub-100 nm Si Thin-Film Transistors by Pattern-Controlled Crystallization of Thin Channel Layer and High Temperature Annealing", DRC Conference Digest, 2002, pp. 49-50.		
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.					

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LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Arup Bhattacharyya	
				FILING DATE February 10, 2003	GROUP 2814
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TD	AM		Feder, B.J., "I.B.M. Finds Way to Speed Up Chips", The New York Times, June 8, 2001, reprinted from		
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	AP		Ernst, T. et al., "Fabrication of a Novel Strained SiGe:C-channel Planar 55 nm nMOSFET for High-Performance		
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	AU		Bae, G.J. et al., "A Novel SiGe-Inserted SOI Structure for High Performance PDSOI CMOSFET", IEDM Tech.		
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				FILING DATE February 10, 2003	GROUP 281 14
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	AY		Tezuka, T. et al., "High-Performance Strained Si-on-Insulator MOSFETs by Novel Fabrication Processes Utilizing Ge-Condensation Technique", 2002 VLSI Tech. Digest of Technical Papers, pp. 96-97.		
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	BD		Current, M.I. et al., "Atomic-Layer Cleaving with Si ₃ Ge ₂ Strain Layers for Fabrication of Si and Ge-Rich SOI Device Layers", 2001 IEEE Internatl. SOI Conf. 10/01, pp. 11-12.		
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	BF		Myers, S.M. et al., "Deuterium Interactions in Oxygen-Implanted Copper", J. Appl. Phys., Vol. 65(1), Jan. 1, 1989, p. 311-321.		
	BG		Saggio, M. et al., "Innovative Localized Lifetime Control in High-Speed IGBT's", IEEE Elec. Dev. Lett., V. 18, No. 7, July 1997, pp. 333-335.		
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LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Arup Bhattacharyya			
				PRIORITY FILING DATE February 10, 2003		GROUP <u>Unknown</u> 2814	
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
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	AF						
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FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
							Yes No
	AL						
	AM						
	AN						
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